IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:	Confirmation No.: 2477
WHITE, et al.	Examiner: Daniel D. Chang
Patent No.: 7,030,647	Art Unit: 2819
Issued: April 18, 2006	REQUEST FOR CERTIFICATE OF CORRECTION UNDER 37 CFR § 1.322
Application No.: 10/708,478	
Filed: March 5, 2004	
For: TECHNIQUES FOR CONFIGURING PROGRAMMABLE LOGIC USING ON-CHIP NONVOLATILE MEMORY	

Attn: Certificate of Corrections Branch
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

  Pursuant to 37 CFR 1.322, Applicant submits a Certificate of Correction correcting printing errors made at the time of printing of the patent. No fee is required for this Certificate. The desired corrections are set forth on enclosed Form PTO/SB/44.

Respectfully submitted,

J. Matthew Zigmant
Reg. No. 44,005

TOWNSEND and TOWNSEND and CREW LLP
Two Embarcadero Center, Eighth Floor
San Francisco, California 94111-3834
Tel: (415) 576-0200
Fax: (415) 576-0300
JMZ:jtc
61055583 v1

UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION

Page _1_ of _1_

PATENT NO.   :   7,030,647

APPLICATION NO.:   10/708,478

ISSUE DATE   :   April 18, 2006

INVENTOR(S)   :   White, et al.

    It is certified that an error appears or errors appear in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

In claim 11, column 14, line 62, please delete "fifth" and insert --seventh--.

In claim 11, column 14, line 62, please delete "sixth" and insert --eighth--.

MAILING ADDRESS OF SENDER (Please do not use customer number below):

        J. Matthew Zigmant
        TOWNSEND AND TOWNSEND AND CREW LLP
        Two Embarcadero Center, Eighth Floor
        San Francisco, CA 94111-3834

61055573 v1